An Examination of Data Based Large Signal Models for Wireless Amplifiers

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Abstract

The validity of the assumptions used to construct a data based large signal GaAs MESFET model is examined for wireless RF power amplification. The compliance of measured S-parameter data to model consistency constraints is calculated for a wide region of the device's I-V plane. Strong compliance is observed at the contour integral point and over localized regions of the I-V plane, but not over extended regions which would be traversed by the dynamic load line of a power amplifier operating in gain compression. These effects are further examined by comparing harmonic balance predictions of the data based model to that of a common analytical large signal GaAs MESFET model and to load pull measurements of power, efficiency, and linearity.

I. Introduction

In the design of GaAs MESFET RF amplifiers targeting wireless applications, such as analog and digital cellular radio telephones, accurate large signal device models are particularly important in realizing optimal amplifier performance in minimum design time. Since wireless products are battery powered, amplifier efficiency is a premium which is often emphasized in the design. Thus, the power amplifier typically operates with the MESFET biased close to cut off (class A/B for enhanced efficiency). Other specifications include gain, output power and linearity which may be defined in terms of two tone third order intermodulation distortion. While better efficiency can be achieved by driving the device deep into gain compression, linearity requirements often limit the input RF voltage to slight levels of gain compression.

The intent of this work is to examine a data based large signal model [1], which is available in a commercial harmonic balance simulator, to predict GaAs MESFET RF power amplifiers characteristics. The accuracy of the model, and possible limitations of the model when applied to GaAs MESFET devices for power amplification, will be examined in the context of assumed model consistency constraints and to the prediction of output power, efficiency, and intermodulation distortion. Harmonic balance simulations are performed using this model and the results are contrasted to both a traditional analytical based large signal GaAs MESFET model and to on wafer load pull measurements.

II. Data Based Large Signal Model - Model A

The data based model is based directly on measured dc and small signal S-parameter data taken at various bias points. Three state functions, the RF frequency drain current, gate charge, and drain charge are calculated by contour integration of intrinsic admittance parameters. In order for the state functions to be independent of the integral path, admittance parameters must satisfy three consistency constraints as described by the following equations (1)-(3), in which e_{1i}, e_{2i}, and e_{2r} are set to zero. In the case that these terms are not zero, three consistency errors are defined.

$$e_{1i} = \frac{\partial \mathrm{Im}Y_{11}^{meas}(V_{gs}, V_{ds})}{\partial V_{ds}} - \frac{\partial \mathrm{Im}Y_{12}^{meas}(V_{gs}, V_{ds})}{\partial V_{gs}} \quad (1)$$

$$e_{2i} = \frac{\partial \mathrm{Im}Y_{21}^{meas}(V_{gs}, V_{ds})}{\partial V_{ds}} - \frac{\partial \mathrm{Im}Y_{22}^{meas}(V_{gs}, V_{ds})}{\partial V_{gs}} \quad (2)$$

$$e_{2r} = \frac{\partial \mathrm{Re}Y_{21}^{meas}(V_{gs}, V_{ds})}{\partial V_{ds}} - \frac{\partial \mathrm{Re}Y_{22}^{meas}(V_{gs}, V_{ds})}{\partial V_{gs}} \quad (3)$$

These consistency constraints were calculated over a wide bias range for a 750 μm GaAs MESFET as illustrated in Figure 1. These results indicate that e_{2r} is the dominant error, which occurs in the drain knee voltage and forward gate voltage regions, and the entire region just above pinch-off. Whereas, the other errors are prominent only in the drain knee voltage region. The effect of consistency errors are related to small signal output conductance and transconductance as shown in Figure 2. A significant difference is noted in the predicted output conductance near pinch off compared to the measured small signal value. On the other hand, good agreement is noted between predicted and measured transconductance in most regions.

III. Analytical Based Large Signal Model - Model B

For comparative purposes, a modified Curtice model (Model B) is also considered [2]. This model has been implemented in a harmonic balance simulator through user developed C

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code routines. Extraction of model parameters is based on previous work [3-4]. From forward biased S-parameter measurements, parasitic resistances Rs, Rd, and Rg are determined. Similarly, ideality factor (N) and saturation current (Is) are obtained from forward dc I-V measurements. Other characterization includes measuring S-parameters and dc I-V over a wide region of the device's I-V plane. At each bias state, FET equivalent circuit elements (gm, gds, Cgs, Cgd, ...) are extracted.

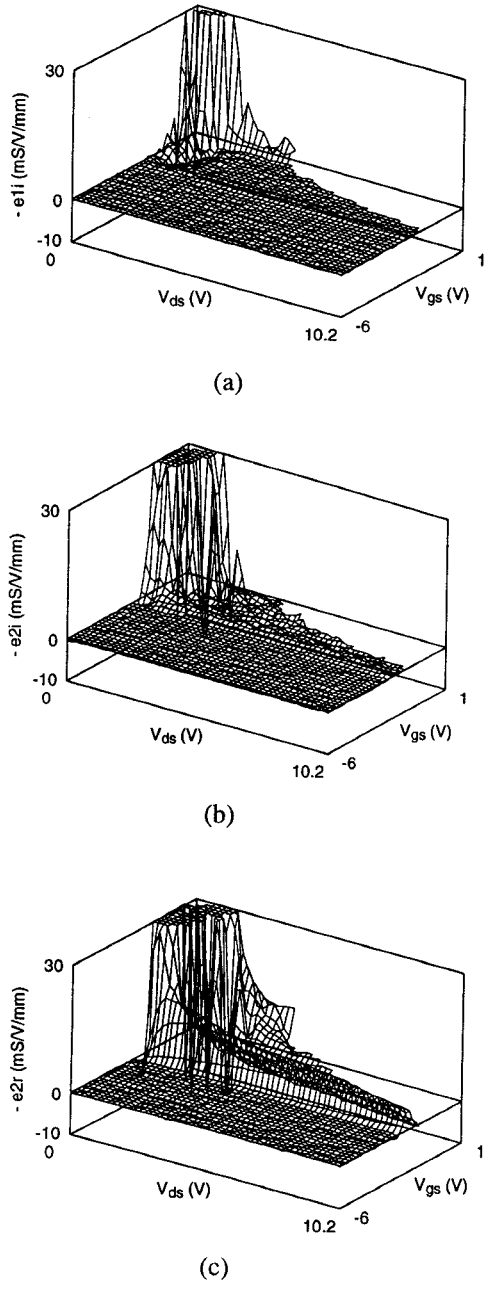


Fig. 1. Imaginary and real component of the consistency error (a) e_{1i}, (b) e_{2i}, and (c) e_{2r}.

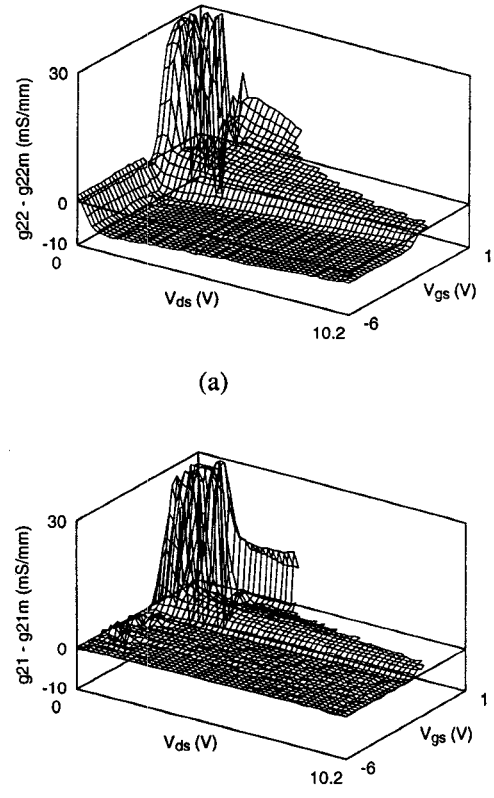


Fig. 2. 3-D plot of the difference between measured and simulated (a) output conductance g_{22} and (b) transconductance g_{21}.

An extraction algorithm then determines large signal model parameter values based on the above data set (RF parameters gm, gds, Tau, Cgs, Cgd, Cds and dc drain current) by minimizing the error between measured and modeled values. Gate-source and gate-drain capacitances are modeled with simple diode junction expressions. Drain-source capacitance Cds is assumed constant

IV. Large Signal Model Verification

The inability of the data based model to match the small signal conductance data and the effect on large signal model predictions is examined for this GaAs MESFET device when used for power amplification. Harmonic balance predictions of output power, efficiency, and intermodulation distortion are compared to analytical model B and to on wafer load pull measurements made on this device.

The load pull system is characterized such that all measurements (output power, efficiency, intermodulation

distortion) are referenced to the device's gate and drain terminal. The source and load tuners and other system components are characterized such that the reflection coefficient presented to the device's gate and drain terminal is precisely known at the fundamental through the fifth harmonic frequency. The harmonic balance simulations incorporate these reflection coefficients such that an accurate representation of the actual measurement system is utilized.

Measurements were performed with the device biased for class A/B operation (~10 % of I_{DSS}). Data was measured at two load states which were selected for device operation with steep and shallow load conductances of $\Gamma_{L@fo} = 0.16\angle 5.8^{\circ}$ and $0.40\angle 1.6^{\circ}$, respectively. Measurements of output power, power added efficiency, and drain current were made with a single tone sinusoidal input stimulus at a frequency of 850 MHz as a function of the available source power. Note that the source power was swept to drive the MESFET from small signal operation to several dB of gain compression. Similarly, intermodulation distortion was measured for input stimuli at frequencies of 849.75 MHz and 850.25 MHz. Again the available input power of the RF source was swept to drive the MESFET into gain compression. The measured results were compared with harmonic balance predictions based on models A and B.

Measured results and model predictions are shown in Figure 3 for a load termination of $\Gamma_{L@fo} = 0.16\angle 5.8^{\circ}$. An inspection of gain and output power shows excellent agreement between the data based model and measured values. The analytical model slightly over predicts small signal gain, but shows excellent agreement under gain compression. Third order intermodulation distortion is generally well predicted by both models although somewhat larger differences are noted at low input power levels with model A. Significant differences are observed between measured drain current/efficiency and that predicted by model A, especially as the device saturates, whereas model B is quantitatively more accurate.

Measured results and model predictions are shown in Figure 4 for the low conductance termination ($\Gamma_{L@fo} = 0.40\angle 1.6^{\circ}$). An inspection of gain and output power shows similar agreement to the previous case. However, drain current is now significantly over predicted by model A when the device operates in gain compression. This poor agreement in modeled efficiency with the data based model is attributed to an over estimated drain current , which in turn originated from the g_{22} over prediction in the device pinch off region as illustrated in Figure 2a. It is believed that the error in drain current prediction is more pronounced for the lower conductance load case. This effect is more readily observed by considering the dynamic load line plotted against the dc I-V curves using Model A as illustrated in Figure 5. At higher

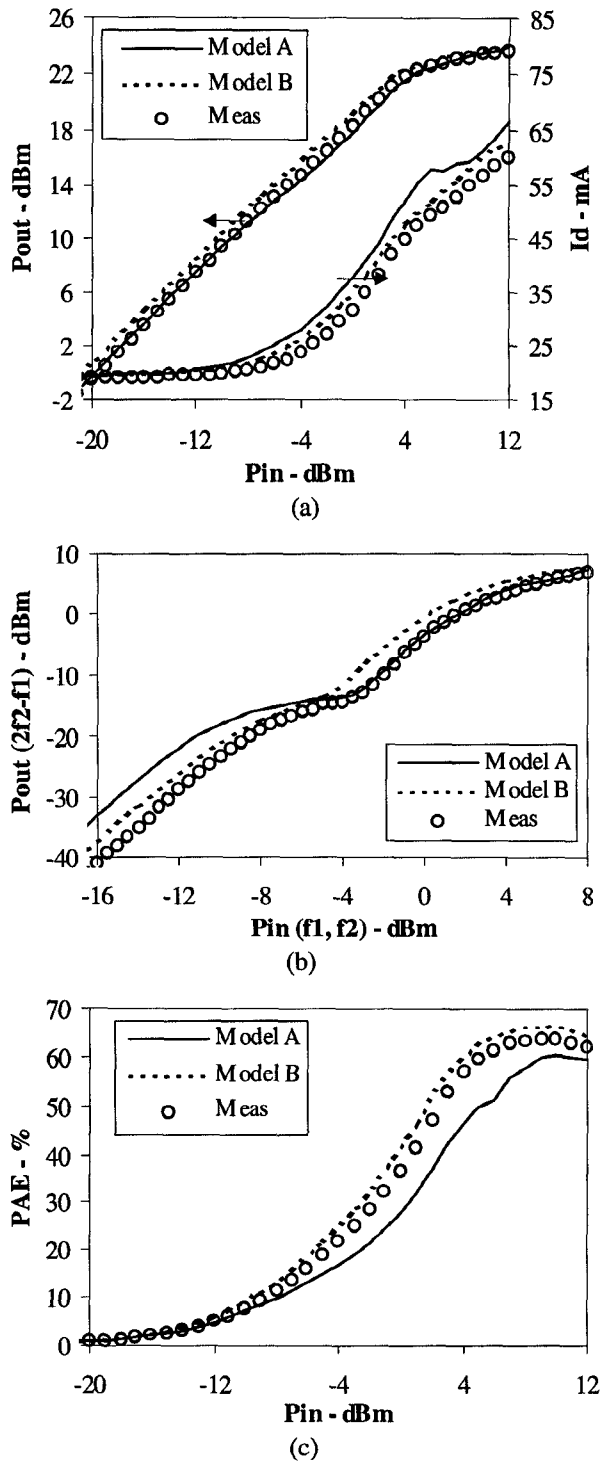
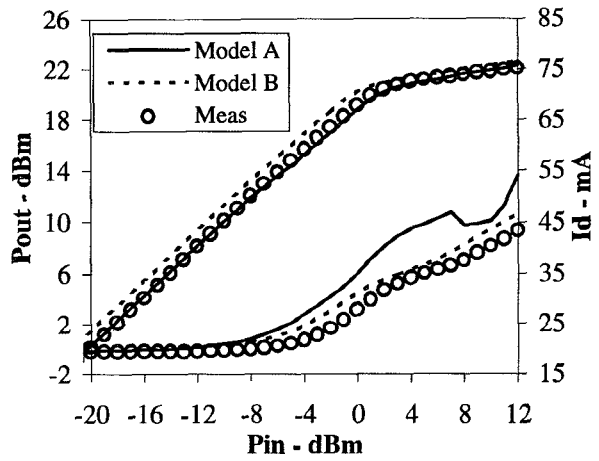
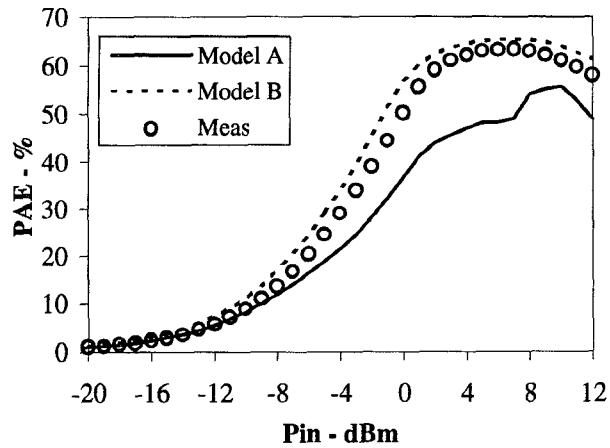


Fig. 3. Predictions from large signal model A are compared to analytical large signal model B and to load pull measurements made on the GaAs MESFET device when terminated with a high conductance load ($\Gamma_{L@fo} = 0.16\angle 5.8^{\circ}$). a) Output power and drain current, b) Two tone third order intermodulation power, and c) Power added efficiency.



(a)



(b)

Fig. 4. Predictions from large signal model A are compared to an analytical large signal model B and to load pull measurements of the GaAs MESFET device terminated in a low conductance load ($\Gamma_{L@fo}$ = 0.40∠1.6°). a) Output power and drain current, and b) Power added efficiency.

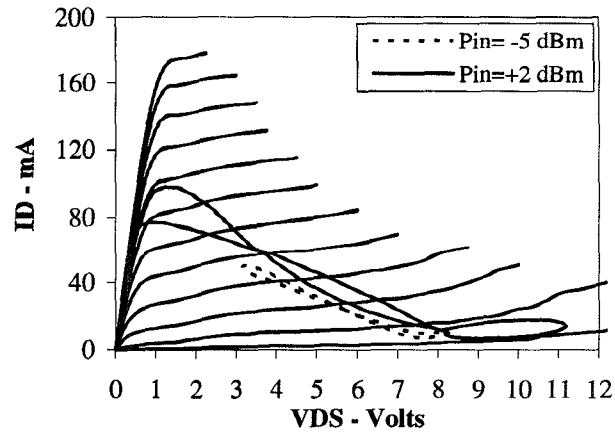


Fig. 5. Predicted dynamic load line for large signal model A ($\Gamma_{L@fo}$ = 0.40∠1.6°).

input power levels where the device begins to exhibit gain compression, the RF current does not approach zero as the RF gate-source voltage (V_{gs}) extends below the device pinch off voltage. This situation becomes more pronounced at higher input RF voltage levels which corresponds to higher gain compression (Fig. 5). In addition, the g_{22} over prediction in the device pinch off region leads to larger errors in predicting efficiency with model A as the load conductance decreases.

V. Summary

In summary, a data based model was evaluated for a 750 μm GaAs MESFET device operating as a class AB power amplifier. Close agreement was obtained in predicting gain, output power, and third order intermodulation distortion. However, a large discrepancy is noted between modeled and measured efficiency, particularly under higher input RF drive conditions. This effect originates from the assumption that the GaAs MESFET device will satisfy the required model consistency constraints over wide region of the devices I-V plane. Computations of the consistency errors for our GaAs MESFET device suggest this is not necessarily met over a wide region of the device's I-V plane. In contrast, the analytical based large signal GaAs MESFET model predicts drain current and efficiency quantitatively much more accurately when compared to the data based model. Conversely, less accurate predictions are noted for small signal gain.

References

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